

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Harold M. Chase, et al. **Examiner:** Unassigned

Serial No.: To Be Assigned **Art Unit:** Unassigned

Filed: Herewith **Docket:** 12675Z

For: METHOD FOR VLSI SYSTEM
DEBUG AND TIMING ANALYSIS **Dated:** September 16, 2003

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

PRELIMINARY AMENDMENT

Sir:

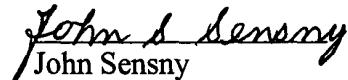
Please amend the subject patent application as follows:

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Dated: September 16, 2003


John Sensny